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SAWYER LAW GROUP LLP
P O BOX 51418
PALO ALTO, CA 94303

EXAMINER	
HSU, JONI	
ART UNIT	**PAPER NUMBER**
2671	

DATE MAILED: 08/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,431	LEWIS, MICHAEL C.	
	Examiner	Art Unit	
	Joni Hsu	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-26 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/10/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-26 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-26 of U.S. Patent No. 6,624,819. Although the conflicting claims are not identical, they are not patentably distinct from each other because independent claims 1 and 14 of U.S. Patent No. 6,624,819 are the same as independent claims 1 and 14 of this application, except that claims 1 and 14 of U.S. Patent No. 6,624,819 have the additional limitation of "wherein the vector co-processor further includes a first data path and a second data path, the first data path including a single operand unit for performing a first plurality of operations on a single input to the vector co-processor, the second data path including a plurality of multipliers and a plurality of adders for performing a second plurality of operations, the single operand unit being in the first data path but not the second data path." Therefore, independent claims 1 and 14 of U.S. Patent No. 6,624,819 cover all of the limitations

of independent claims 1 and 14 of this application. Dependent claims 2-13 and 15-26 of U.S. Patent No. 6,624,819 are substantially the same as dependent claims 2-13 and 15-26 of this application.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on July 10, 2003 was filed after the mailing date of the application on July 10, 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

4. Claim 24 objected to because of the following informalities: Claim 24 recites "wherein vector co-processor further a first vector buffer..." where it should recite "wherein vector co-processor further **includes** a first vector buffer...". Claim 24 also recites "(b1) obtaining...direct memory access unit" where it should recite "(b1) obtaining...direct memory access unit;". Claim 24 also recites "(b2) providing...the first vector buffer and **a** the second vector buffer;" where it should recite "(b2) providing...the first vector buffer and the second vector buffer;". Claim 24 also recites "(b**4**) providing...includes instructions for...adder tree" where it should recite "(b**5**) providing...includes instructions for...adder tree;", and (b5) should be changed to (b6). Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4, 13-17, and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Lindholm (US006417851B1).

7. With regard to Claim 1, Lindholm describes a system for processing graphics data in a computer system (*graphics processors*, Col. 1, lines 32-34) comprising a general-purpose processor (*microcontroller or CPU*, Col. 5, lines 64-67) including an instruction queue (452, Figure 4B), the instruction queue for holding a plurality of instructions (Col. 10, lines 21-54); a vector co-processor (52, 54, 56, Figure 1A), coupled with the general-purpose processor, for processing at least a portion of the graphics data using a portion of the plurality of instructions (Col. 5, lines 26-37, 60-67), the vector co-processor capable of performing a plurality of mathematical operations in parallel (*transform module 52 processing in parallel*, Col. 9, lines 18-21), the plurality of instructions being written in a general-purpose programming language (*employs Open GL, OpenGL is the computer industry's standard application program interface for defining 2-D and 3-D graphic images*, Col. 5, lines 38-48).

8. With regard to Claim 2, Lindholm describes that the plurality of mathematical operations are a plurality of multiply operations and wherein the vector co-processor (52, 54, 56, Figure 1A; Col. 5, lines 26-37) further includes a plurality of multipliers (600, Figure 6) for performing the plurality of multiply operations in parallel (*MLU 500 of the transform module 52 includes four multipliers 600 that are coupled in parallel*, Col. 11, lines 61-65).

9. With regard to Claim 3, Lindholm describes that the plurality of multipliers (600, 500, Figure 6) provide a first plurality of resultants (Col. 11, lines 61-65) and wherein the vector co-processor (52, 54, 56, Figure 1A; Col. 5, lines 26-37) further includes an adder tree (700, Figure 7; 504, Figure 5; *ALU 504 of transform module 52 includes three adders 700 coupled in parallel/series*, Col. 12, lines 40-48), coupled to the plurality of multipliers (*ALU 504 having a first input coupled to an output of MLU 500*, Col. 11, lines 15-16), including at least one stage, the adder tree for adding at least a portion of the first plurality of resultants; a plurality of resultant paths (O[4], Figures 6, 7) coupled with the plurality of multipliers and the adder tree for providing the plurality of resultants from the plurality of multipliers (Col. 12, lines 1-15) or a second plurality of resultants from the at least one stage of the adder tree (*ALU 504 can add two three component vectors, pass one four component vector, or smear a vector component across the output*, Col. 12, lines 40-63), as shown in Figures 6 and 7.

10. With regard to Claim 4, Lindholm describes that the vector co-processor (52, 54, 56, Figure 1A; Col. 5, lines 26-37) further includes a first vector buffer and a second vector buffer (400, Figure 4; *transform module 52 is connected to VAB 40 by way of 6 input buffers 400*, Col.

8, lines 55-62), wherein the vector co-processor can perform the plurality of mathematical operations on a first portion of the graphics data from the first vector buffer (buffer in the allocated state) while a second portion of the graphics data is being provided to the second vector buffer (buffer in the valid state) (*if a buffer/slot is in the valid state, the buffer/slot is available for receiving vertex data, the active state indicates that a buffer/slot is currently in an execution state*, Col. 25, lines 48-56, *upon receiving vertex data in one of the first set of buffers 400, such buffer is placed in the valid state, after which one of the second set of buffers 402, 404 is placed in the allocated state in anticipation of the output of transform module 52*, Col. 25, lines 58-62) and wherein the vector co-processor can perform the plurality of mathematical operations on the second portion of the graphics data from the second vector buffer while the first portion of the graphics data is being provided to the first vector buffer (*after one of the second set of buffers 404, 406 is placed in the allocated state, the buffer of the first set 400 is placed in the active state. When transform module 52 is finished execution, the buffer of the second set 404, 406 is read and then placed in the valid state*, Col. 26, lines 4-10).

11. With regard to Claim 13, Lindholm describes that the vector co-processor (52, 54, 56, Figure 1A) is capable of performing transformations, clipping (*clipping operations to be handled by rasterization module 56*, Col. 14, lines 35-37) and a determination of at least one lighting value for the at least portion of the graphics data (*transform module 52 generates vectors for lighting module 54*, Col. 5, lines 28-37).

12. With regard to Claim 14, Claim 14 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

13. With regard to Claim 15, Claim 15 is similar in scope to Claim 2, and therefore is rejected under the same rationale.

14. With regard to Claim 16, Lindholm describes that the plurality of multipliers (600, 500, Figure 6) provide a first plurality of resultants (Col. 11, lines 61-65) and wherein the vector co-processor (52, 54, 56, Figure 1A; Col. 5, lines 26-37) further includes an adder tree (700, Figure 7; 504, Figure 5; Col. 12, lines 12-48) including at least one stage coupled to the plurality of multipliers (Col. 11, lines 15-16) and a plurality of resultant paths (O[4], Figures 6, 7) coupled to the plurality of multipliers and the at least one stage of the adder tree. The adder operates according to the instructions it receives (*instructions used to operate adder 456*, Col. 10, lines 25-27). Therefore, the processing step (b) further includes the step of adding a first portion of the first plurality of resultants utilizing the adder tree if plurality of instructions includes instructions for adding the first portion of the plurality of resultants (CALU_ADDB, Col. 12, lines 40-64); and providing the plurality of resultants from the plurality of multipliers (CALU_PASB; *ALU 504 can pass one four component vector*, Col. 12, lines 40-64) or a second plurality of resultants from the at least one stage of the adder tree (CALU_SUM3B; *ALU 504 can add two three component vectors*, Col. 12, lines 40-64) if the plurality of instructions includes instructions for providing the plurality of resultants from the plurality of multipliers or

the second plurality of resultants from the at least one stage of the adder tree (Col. 12, lines 40-64).

15. With regard to Claim 17, Lindholm describes that the vector co-processor (52, 54, 56, Figure 1A; Col. 5, lines 26-37) further includes a first vector buffer and a second vector buffer (400, Figure 4; Col. 8, lines 55-62), wherein the processing step (b) further includes the steps of providing a portion of the graphics data alternately to the first vector buffer and the second vector buffer; utilizing the vector co-processor to perform the plurality of mathematical operations on a first portion of the graphics data from the first vector buffer (buffer in the allocated state) while a second portion of the graphics data is being provided to the second vector buffer (buffer in the valid state) (Col. 25, lines 48-62) and to perform the plurality of mathematical operations on the second portion of the graphics data from the second vector buffer while the first portion of the graphics data is being provided to the first vector buffer (Col. 26, lines 4-10).

16. With regard to Claim 26, Claim 26 is similar in scope to Claim 13, and therefore is rejected under the same rationale.

17. Thus, it reasonably appears that Lindholm describes or discloses every element of Claims 1-4, 13-17, and 26 and therefore anticipates the claims subject.

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

20. Claims 5-12, and 18-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lindholm (US006417851B1) in view of Ohba (US006427201B1).

21. With regard to Claim 5, Lindholm is relied upon for the teachings as discussed above relative to Claim 1.

However, Lindholm does not teach that the vector co-processor further includes a direct memory access unit for obtaining data directly from a memory. However, Ohba describes the vector co-processor further includes a direct memory access unit for obtaining data directly from a memory (*vector processor having a data transfer mechanism by DMA*, Col. 2, lines 56-65).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Lindholm so that the vector co-processor further includes a direct memory access unit for obtaining data directly from a memory as suggested by Ohba. Direct memory access can control the memory system without using the CPU, and is much faster than using the CPU to manage the transfers. Direct memory access is well-known in the art, widely used, and can be found in many publications, such as Ganier's website.

22. With regard to Claim 6, Lindholm does not specifically teach that the memory includes a system memory. However, Ohba describes that the memory includes a system memory (*DMAC 14 intelligently distributes data as it arbitrates the main bus for plural processors which use the main memory resources*, Col. 4, lines 62-67).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Lindholm so that the memory includes a system memory as suggested by Ohba because Ohba suggests that access to the system memory is needed in order to obtain the programs to be executed (Col. 7, lines 29-39).

23. With regard to Claim 7, Lindholm does not specifically teach that the memory includes local memory. However, Ohba describes that the memory includes a local memory (*direct memory-accessible high-speed internal storage means*, Col. 2, lines 45-49).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Lindholm so that the memory includes local memory as suggested by Ohba because Ohba suggests that the local memory is a high-speed internal

memory, and this memory is needed in order to process routine data efficiently (Col. 2, lines 45-49).

24. With regard to Claim 8, Lindholm does not specifically teach that the vector co-processor is capable of processing the at least the portion of the graphics data while the general-purpose processor performs a plurality of other operations. However, Ohba describes that the vector co-processor is capable of processing the at least the portion of the graphics data (routine processing) while the general-purpose processor (20) performs a plurality of other operations (non-routine processing) (*main CPU 20 generates data for non-routine processing (polygon definition)*, Col. 6, lines 1-7; vector processor for routine processing of routine data, Col. 2, lines 45-65).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Lindholm so that the vector co-processor is capable of processing the at least the portion of the graphics data while the general-purpose processor performs a plurality of other operations as suggested by Ohba because Ohba suggests that routine and non-routine processing can be performed efficiently at the same time (Col. 2, lines 49-55).

25. With regard to Claim 9, Lindholm does not teach that the plurality of other operations further include processing a second portion of the graphics data. However, Ohba describes that the plurality of other operations further include processing a second portion of the graphics data (*main CPU 20 generates data for non-routine processing (polygon definition)*, Col. 6, lines 1-7). This would be obvious for the same reasons given in the rejection for Claim 8.

26. With regard to Claim 10, Lindholm does not teach that the plurality of other operations are used in processing the graphics data. However, Ohba describes that the plurality of other operations are used in processing the graphics data (Col. 6, lines 1-7). This would be obvious for the same reasons given in the rejection for Claim 8.

27. With regard to Claim 11, Lindholm describes that the plurality of operations are a plurality of multiplies (600, Figure 6; Col. 11, lines 61-65), wherein vector co-processor (52, 54, 56, Figure 1A; Col. 5, lines 28-37) further includes a first vector buffer and a second vector buffer (400, Figure 4; Col. 8, lines 56-58), wherein the vector co-processor can perform the plurality of mathematical operations on a first portion of the graphics data from the first vector buffer (buffer currently in an execution state) while a second portion of the graphics data is being provided to the second vector buffer (buffer in a valid state) and wherein the vector co-processor can perform the plurality of mathematical operations on the second portion of the graphics data from the second vector buffer (buffer currently in an execution state) while the first portion of the graphics data is being provided to the first vector buffer (buffer in a valid state) (Col. 25, lines 48-56); a plurality of multipliers (600, Figure 6, 500, Figure 5; Col. 11, lines 61-65), coupled with the first vector buffer and the second vector buffer (Col. 11, lines 11-12), for performing the plurality of multiply operations in parallel to provide a first plurality of resultants (Col. 11, lines 61-65); an adder tree (700, Figure 7, 504, Figure 5; Col. 12, lines 42-44), coupled to the plurality of multipliers (Col. 11, lines 15-16), including at least one stage, the adder tree for adding at least a portion of the first plurality of resultants; a plurality of resultant paths

(O[4]), coupled to the plurality of multipliers and the adder tree, for providing the plurality of resultants from the plurality of multipliers and the adder tree, for providing the plurality of resultants from the plurality of multipliers or a second plurality of resultants from the at least one stage of the adder tree (Col. 12, lines 1-15, 40-63), as shown in Figures 6 and 7. Lindholm describes a resultant mask (510) coupled with the plurality of resultant paths (*unmasked components would be taken from the registers and masked components would be bypassed, vector register file 510 is thus very useful for building up vectors component by component, or for changing the order of vector components in conjunction with the ALU SMR operations*, Col. 13, lines 38-44, 16-45), the first vector buffer and the second vector buffer (Col. 5, lines 10-27), as shown in Figure 5. The first and the second buffer access the vertex attribute buffer (50; *input buffers 400 are coupled to VAB 50 for receiving vertex data therefrom*, Col. 11, lines 7-9).

However, Lindholm does not specifically teach that the system further includes a memory and a direct memory access unit, coupled with the first buffer and the second buffer, for accessing a memory. However, Ohba describes that the system further includes a memory (50, Figure 1) and a direct memory access unit (14) for accessing a memory (Col. 3, lines 46-49). This would be obvious for the same reasons given in the rejections of Claims 5 and 6.

28. With regard to Claim 12, according to the disclosure of this application, a single operand unit performs single input operations, such as reciprocals and square roots (page 14, lines 19-20). Lindholm describes that the vector co-processor (52, 54, 56, Figure 1A; Col. 5, lines 28-37) further includes a single operand unit (512), coupled with the first vector buffer and the second vector buffer (400) (Col. 11, lines 10-11, 15-16, 22-27), for performing a plurality of operations

(reciprocals, square roots) on a single input from the first vector buffer or the second vector buffer (*ILU 512 is provided for performing an inverse square root operation*, Col. 11, lines 23-27; *ILU 512 of transform module 52 is capable of generating a reciprocal and a reciprocal square root*, Col. 13, lines 45-50).

29. With regard to Claim 18, Claim 18 is similar in scope to Claim 5, and therefore is rejected under the same rationale.

30. With regard to Claim 19, Claim 19 is similar in scope to Claim 6, and therefore is rejected under the same rationale.

31. With regard to Claim 20, Claim 20 is similar in scope to Claim 7, and therefore is rejected under the same rationale.

32. With regard to Claim 21, Claim 21 is similar in scope to Claim 8, and therefore is rejected under the same rationale.

33. With regard to Claim 22, Claim 22 is similar in scope to Claim 9, and therefore is rejected under the same rationale.

34. With regard to Claim 23, Claim 23 is similar in scope to Claim 10, and therefore is rejected under the same rationale.

35. With regard to Claim 24, Lindholm describes that the plurality of operations are a plurality of multiplies (600, Figure 6; Col. 11, lines 61-65), wherein vector co-processor (52, 54, 56, Figure 1A) further includes a memory (50) (Col. 5, lines 26-37) and wherein vector co-processor further includes a first vector buffer, a second vector buffer (400, Figure 5), a plurality of multipliers (600, Figure 6; 500, Figure 5; Col. 11, lines 61-65) coupled to the first vector buffer and the second vector buffer (Col. 11, lines 10-11), an adder tree (504, Figure 7; Col. 12, liens 40-48) including at least one stage coupled with the plurality of multipliers (Figure 5; Col. 11, lines 15-16), a plurality of resultant paths coupled to the plurality of multipliers and the adder tree (O[4], Col. 12, lines 1-63), as shown in Figures 6 and 7. A resultant mask (510) is coupled with the plurality of resultant paths (Col. 13, lines 16-45), the first vector buffer and the second vector buffer (Col. 11, lines 10-27), as shown in Figure 5. The first vector buffer and the second vector buffer are coupled to the vertex attribute buffer (50) to obtain a portion of the graphics data (Col. 11, lines 7-9). The method includes the steps of providing the portion of the graphics data alternatively to the first vector buffer and the second vector buffer; performing the plurality of operations on a first portion of the graphics data from the first vector buffer (allocated buffer) while a second portion of the graphics data is being provided to the second vector buffer (valid buffer) (Col. 25, lines 48-62) and to perform the plurality of operations on the second portion of the graphics data from the second vector buffer while the first portion of the graphics data is being provided to the first vector buffer (Col. 26, lines 4-10). The plurality of operations are performed by the multipliers, the plurality of multipliers thereby providing a plurality of resultants (Col. 11, line 61-Col. 12, line 15). The adder operates according to the instructions it

receives (Col. 10, lines 25-27). Therefore, Lindholm discloses adding a first portion of the first plurality of resultants utilizing the adder tree if plurality of instructions includes instructions for adding the first portion of the plurality of resultants (CALU_ADDB); and providing a second portion of the plurality of resultants from the plurality of multipliers or a second plurality of resultants from the at least one stage of the adder tree if the plurality of instructions includes instructions for providing the plurality of resultants from the plurality of multipliers or the second plurality of resultants from the at least one stage of the adder tree (CALU_SUM3B) (Col. 12, lines 40-63). The vector co-processor operates according to the instructions it receives (Col. 10, lines 25-27), and the vector co-processor operations on the plurality of resultants determined by the mask (Col. 13, lines 16-45). The mask determines which components would be taken from the register and which components would be bypassed for processing in the vector co-processor (Col. 13, lines 16-45). The vector co-processor processes data from the first vector buffer and the second vector buffer (Col. 11, lines 10-11). Therefore, Lindholm discloses utilizing the mask to provide the second portion of the plurality of resultants or the second plurality of resultants to the first vector buffer or the second vector buffer if a portion of the plurality of instructions indicate that the second portion of the plurality of resultants or the second plurality of resultants are to be provided to the first vector buffer or the second vector buffer.

However, Lindholm does not specifically teach that the system further includes a memory, a direct memory access unit coupled with the first vector buffer and the second vector buffer, the method including the step of obtaining a portion of the graphics data directly from a memory of the system utilizing the direct memory access unit. However, Obha describes that the

system further includes a memory (50, Figure 1), a direct memory access unit (14), the method including the step of obtaining a portion of the graphics data directly from a memory of the system (Col. 6, lines 11-18) utilizing the direct memory access unit (Col. 4, lines 62-64). This would be obvious for the same reasons given in the rejections of Claims 5 and 6.

36. With regard to Claim 25, Lindholm describes that the vector co-processor (52, 54, 56, Figure 1A; Col. 5, lines 28-37) further includes a single operand unit (512) coupled with the first vector buffer and the second vector buffer (400) (Col. 11, lines 10-11, 15-16, 22-27), the method further comprising the step of performing a plurality of operations (reciprocals, square roots) on a single input from the first vector buffer or the second vector buffer (Col. 11, lines 23-27; Col. 13, lines 45-50). Lindholm describes that the single operand unit operates according to instructions (*instructions used to operate inverse logic unit*, Col. 10, lines 25-27). Therefore, the single operand unit performs these operations if a second portion of the plurality of instructions indicates that the plurality of operations are to be performed on the single input.

Prior Art of Record

Ganier, C.J. "What is Direct Memory Access (DMA)?"
http://cnx.rice.edu/content/m11867/latest/.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

Kee M. Tung
Primary Examiner